IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
HENDERSON ET AL.)
)
Serial No. **Not Yet Assigned**)
)
Filing Date: **Herewith**)
)
For: **MODIFICATION OF COLUMN FIXED**)
PATTERN NOISE IN SOLID STATE)
IMAGE SENSORS)
)

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EXPRESS MAIL NO: EL747059351US

DATE OF DEPOSIT: August 17, 2001

NAME: Regan Sampson

SIGNATURE: Regan Sampson

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to correct the spelling of a translated word in FIGS. 1 and 3. FIG. 8 is also being modified as indicated in red ink to remove an extraneous marking therefrom.

In the Claims:

Please cancel Claims 1 to 18.

Please add new Claims 19 to 57.

19. A method of operating a solid state image sensor

comprising an array of photosensitive pixels arranged in rows and columns and in which pixel data signals are read therefrom via corresponding column circuits that introduce column fixed pattern noise to the pixel data signals, the method comprising:

selectively inverting the pixel data signals being input to the column circuits; and

reversing the inversion of the inverted pixel data signals following output from the column circuits.

20. A method according to Claim 19, wherein each column circuit comprises:

an analog-to-digital converter; and

a digital inverter connected to said analog-to-digital converter for selectively inverting digital output signals therefrom.

21. A method according to Claim 19, wherein the selectively inverting is applied to alternate rows of the pixel data signals.

22. A method according to Claim 19, wherein the selectively inverting is applied to alternate groups of rows of the pixel data signals.

23. A method according to Claim 22, wherein the selectively inverting is applied to alternate pairs of rows of the pixel data signals in the alternate groups of rows.

24. A method according to Claim 19, wherein the selectively inverting is applied differently to different

frames of the pixel data signals.

25. A method according to Claim 24, wherein the selectively inverting comprises:

applying a first selective inversion scheme to alternate frames; and

applying a second selective inversion scheme opposite to the first selective inversion scheme to intervening frames.

26. A method according to Claim 19, further comprising selectively switching outputs from adjacent columns between adjacent column output channels prior to selectively inverting the pixel data signals input to the column circuits.

27. A method of operating a solid state image sensor comprising an array of photosensitive pixels arranged in rows and columns, the method comprising:

reading pixel data signals from the array of photosensitive pixels via corresponding column circuits;

selectively inverting the pixel data signals being input to the column circuits; and

reversing the inversion of the inverted pixel data signals following output from the column circuits.

28. A method according to Claim 27, wherein each column circuit comprises:

an analog-to-digital converter; and

a digital inverter connected to said analog-to-digital converter for selectively inverting digital output signals therefrom.

29. A method according to Claim 27, wherein the selectively inverting is applied to alternate rows of the pixel data signals.

30. A method according to Claim 27, wherein the selectively inverting is applied to alternate groups of rows of the pixel data signals.

31. A method according to Claim 30, wherein the selectively inverting is applied to alternate pairs of rows of the pixel data signals in the alternate groups of rows.

32. A method according to Claim 27, wherein the selectively inverting is applied differently to different frames of the pixel data signals.

33. A method according to Claim 32, wherein the selectively inverting comprises:

applying a first selective inversion scheme to alternate frames; and

applying a second selective inversion scheme opposite to the first selective inversion scheme to intervening frames.

34. A method according to Claim 27, further comprising selectively switching outputs from adjacent columns between adjacent column output channels prior to selectively inverting the pixel data signals input to the column circuits.

35. A solid state image sensor comprising:

an array of photosensitive pixels arranged in rows and columns;

a plurality of column circuits connected to the columns of said array of photosensitive pixels for reading pixel data signals therefrom while introducing column fixed pattern noise to the pixel data signals;

inverting means for selectively inverting the pixel data signals input to said plurality of column circuits; and

reversing means for reversing the inversion of the inverted pixel data signals following output from said plurality of column circuits.

36. A solid state image sensor according to Claim 35, wherein said inverting means comprises a first chopping circuit at an input of each column circuit.

37. A solid state image sensor according to Claim 35, wherein said array of photosensitive pixels comprises active pixels in which pixel signal voltages and reset voltages are input to said plurality of column circuits; and wherein said inverting means comprises switch means and control means associated therewith for sampling the pixel signal voltages and reset voltages.

38. A solid state image sensor according to Claim 35, wherein said reversing means comprises at least one output chopper circuit.

39. A solid state image sensor according to Claim 38, wherein said at least one output chopper circuit comprises a plurality of output chopper circuits, with each column having an output chopper circuit connected thereto.

40. A solid state image sensor according to Claim 39, wherein each column circuit comprises analog-to-digital conversion means; and wherein each output chopper circuit comprises digital inversion means.

41. A solid state image sensor according to Claim 35, wherein said inverting means and said reversing means are controlled by a common chopping signal.

42. A solid state image sensor according to Claim 35, further comprising switching means for selectively switching outputs from adjacent columns between adjacent column output channels prior to said inverting means selectively inverting the pixel data signals being input to said plurality of column circuits.

43. A solid state image sensor comprising:

an array of photosensitive pixels arranged in rows and columns;

a plurality of column circuits connected to the columns of said array of photosensitive pixels for reading pixel data signals therefrom;

at least one input chopping circuit for selectively inverting the pixel data signals input to said plurality of column circuits; and

at least one output chopping circuit for reversing the inversion of the inverted pixel data signals following output from said plurality of column circuits.

44. A solid state image sensor according to Claim 43, wherein said at least one input chopping circuit comprises

a plurality of input chopping circuits, with an input of each column having an input chopping circuit connected thereto.

45. A solid state image sensor according to Claim 43, wherein said array of photosensitive pixels comprises active pixels in which pixel signal voltages and reset voltages are input to said plurality of column circuits; and wherein said at least one chopping circuit comprises at least one switch and a control circuit associated therewith for sampling the pixel signal voltages and reset voltages.

46. A solid state image sensor according to Claim 43, wherein said at least one output chopper circuit comprises a plurality of output chopper circuits, with each column having an output chopper circuit connected thereto.

47. A solid state image sensor according to Claim 46, wherein each column circuit comprises an analog-to-digital convertor; and wherein each output chopper circuit comprises an invertor.

48. A solid state image sensor according to Claim 43, wherein said at least one input and output chopping circuits are controlled by a common chopping signal.

49. A solid state image sensor according to Claim 43, further comprising a switching circuit for selectively switching outputs from adjacent columns between adjacent column output channels prior to said at least one input chopping circuit selectively inverting the pixel data signals being input to said plurality of column circuits.

50. An imaging system comprising:

a solid state image sensor comprising

an array of photosensitive pixels arranged in rows and columns,

a plurality of column circuits connected to the columns of said array of photosensitive pixels for reading pixel data signals therefrom,

at least one input chopping circuit for selectively inverting the pixel data signals input to said plurality of column circuits, and

at least one output chopping circuit for reversing the inversion of the inverted pixel data signals following output from said plurality of column circuits.

51. An imaging system according to Claim 50, wherein said at least one input chopping circuit comprises a plurality of input chopping circuits, with an input of each column having an input chopping circuit connected thereto.

52. An imaging system according to Claim 50, wherein said array of photosensitive pixels comprises active pixels in which pixel signal voltages and reset voltages are input to said plurality of column circuits; and wherein said at least one input chopping circuit comprises at least one switch and a control circuit associated therewith for sampling the pixel signal voltages and reset voltages.

53. An imaging system according to Claim 50, wherein said at least one output chopper circuit comprises a plurality of output chopper circuits, with each column having an output

chopper circuit connected thereto.

54. An imaging system according to Claim 53, wherein each column circuit comprises an analog-to-digital convertor; and wherein each output chopper circuit comprises an invertor.

55. An imaging system according to Claim 50, wherein said at least one input and output chopping circuits are controlled by a common chopping signal.

56. An imaging system according to Claim 50, wherein said solid state image sensor further comprises a switching circuit for selectively switching outputs from adjacent columns between adjacent column output channels prior to said at least one input chopping circuit selectively inverting the pixel data signals being input to said plurality of column circuits.

57. An imaging system according to Claim 50, wherein the imaging system is configured as a camera.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully

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requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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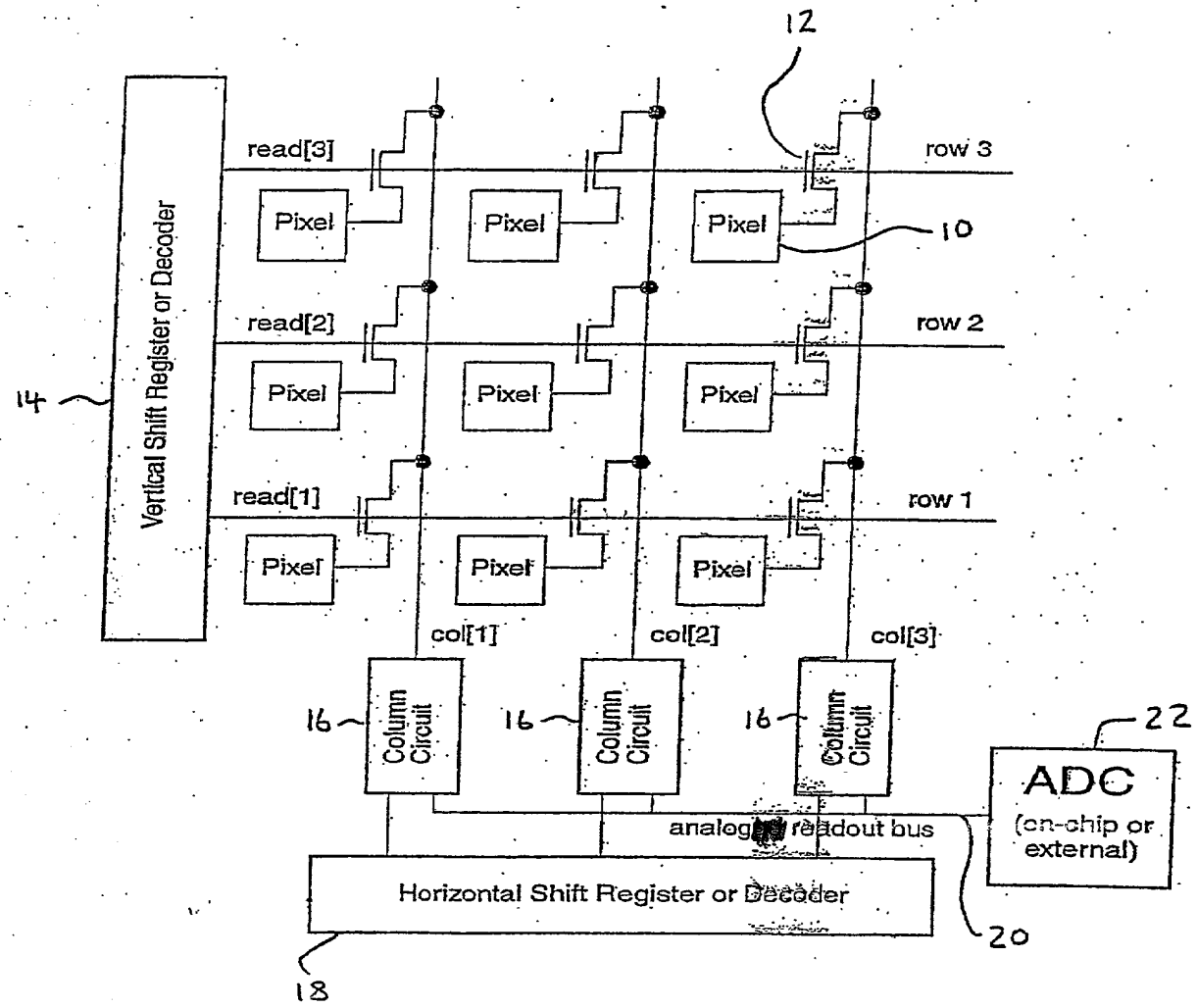

FIG. 1 (PRIOR ART)

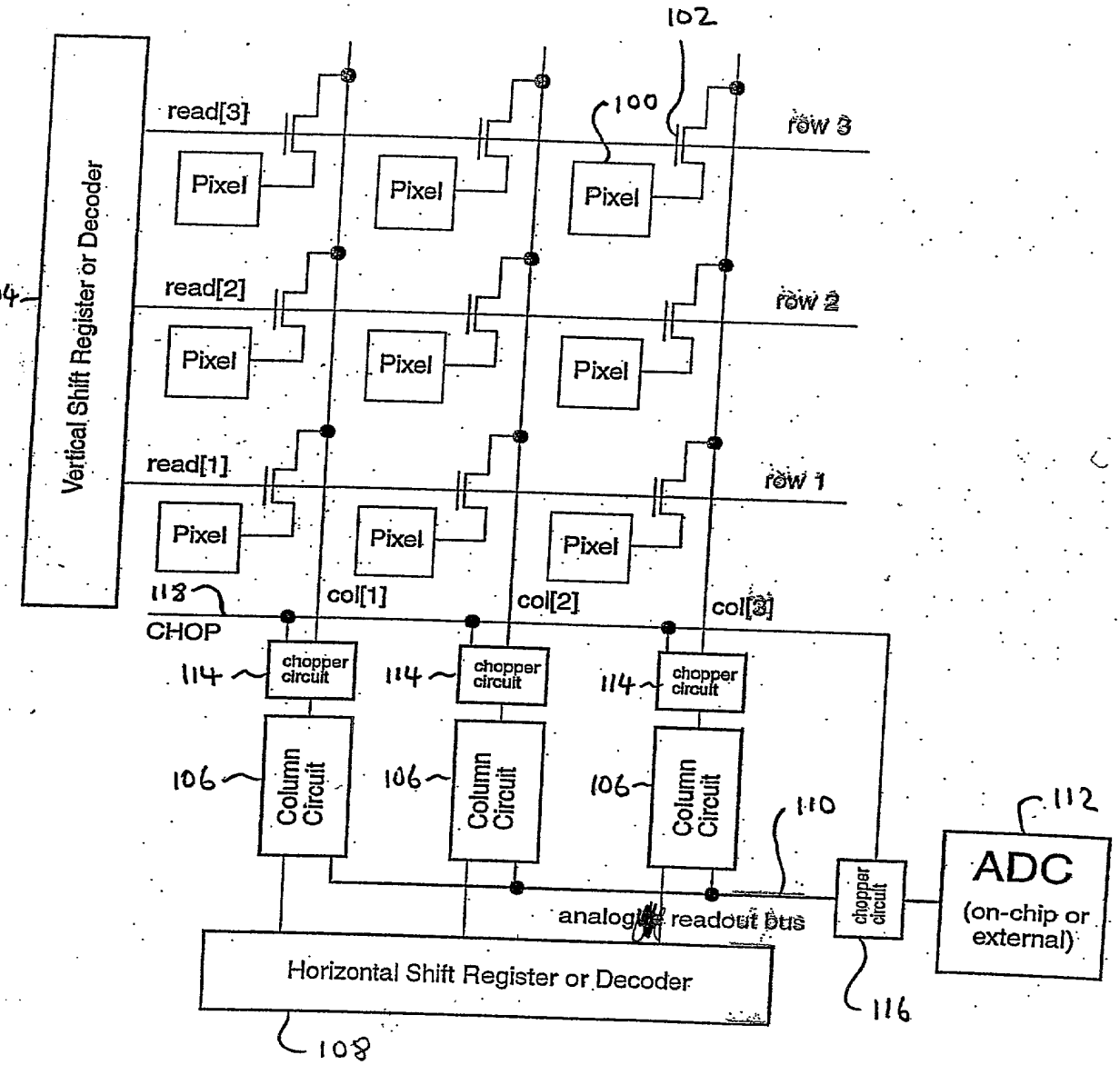
102
100
read[3]
row 3
Pixel
Pixel
Pixel
read[2]
row 2
Pixel
Pixel
Pixel
read[1]
row 1
Pixel
Pixel
Pixel
Vertical Shift Register or Decoder
104
118
CHOP
col[1]
col[2]
col[3]
chopper circuit
114
chopper circuit
114
chopper circuit
114
106
Column Circuit
106
Column Circuit
106
Column Circuit
110
112
ADC
(on-chip or external)
chopper circuit
analog readout bus
Horizontal Shift Register or Decoder
116
108

Fig. 3

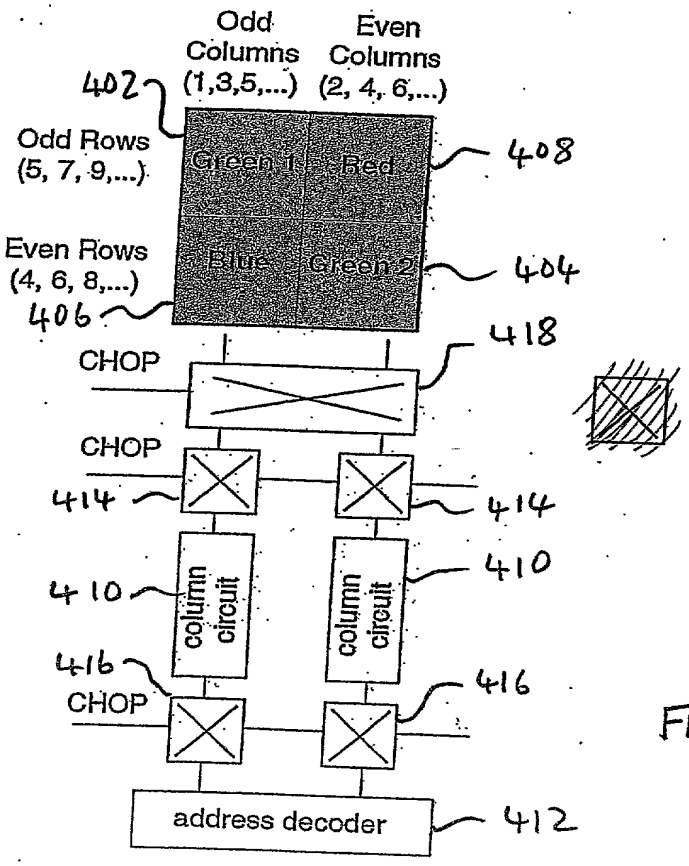
Odd Columns (1,3,5,...)
Even Columns (2, 4, 6,...)
402
Odd Rows (5, 7, 9,...)
Green 1
Red
408
Even Rows (4, 6, 8,...)
Blue
Green 2
404
406
418
CHOP
CHOP
414
414
410
column circuit
column circuit
410
416
CHOP
416
address decoder
412

FIG. 8